Hall Ticket Number:

Code No. : 15446 S O

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E.) V-Semester Supplementary Examinations, June-2023

Computer Organization and Architecture

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Differentiate between Computer Architecture and Organization.	2	2	1	1
2.	Convert (2A5) in to Decimal and Binary representation.	2	3	1	2
3.	Define Stored Program Concept.	2	1	2	1
4.	Write any Two differences between Hardwired and Micro Programmed Control Units.	2	2	2	2
5.	Write the advantages and applications of Vector Processors.	2	2	3	2
6.	List the differences between RISC and CISC?	2	2	3	2
7.	Identify the requirement of I/O Interface.	2	1	4	2
8.	Draw the Diagram for Daisy Chain Priority Interrupt.	2	1	4	2
9.	What is the need for Secondary Memory in a Computer?	2	1	5	2
10.	How many 1024 X 32 RAM Chips are needed to design a Memory Capacity of 64 K Bytes? What is the Size of Address Bus?	2	3	5	3
	Part-B (5 × 8 = 40 Marks)				
11. a)	Perform Booth's multiplication of (-10) and (-6) using algorithm and explain the flow chart.	4	3	1	3
b)	Perform Addition and Multiplication of Two Floating Point Numbers (21.75) and (0.0157). Show the result in normalized representation.	4	4	1	3
12. a)	Draw the Block Diagram of Hard wired control unit and explain it.	4	1	2	1
b)	Explain the importance of interrupt and Hold signals of 8085.	4	2	2	2
13. a)	Explain Arithmetic pipeline with the help an example.	4	2	3	1
b)	Analyze different types of Pipeline Hazards and their remedies.	4	3	3	2

Contd... 2

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14. a)	What are the different types of Asynchronous Data Transfer Methods? Elaborate any one of them.	4	2	4	1
b)	Draw DMA Controller Block Diagram and explain its working.	4	1	4	2
15. a)	What is the need for Memory Hierarchy in Computer Organization? Draw the Structure of Memory Hierarchy.	4	2	5	1
b)	Explain the concept of Associative Memory in detail?	4	2	5	1
16. a)	Explain the hardware requirement for Signed magnitude addition /subtraction algorithm.	4	3	1	1
b)	Classify different instructions of 8085 Microprocessor.	4	2	2	2
17.	Answer any ***two*** of the following:				
a)	A non pipeline system takes 60 ns to perform a task. The same task can be processed in a Four segment pipeline with a clock cycle of 10ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?	4	4	3	3
b)	Derive the circuit for parallel priority interrupt hardware for a system with Four interrupt sources and Explain it.	4	3	4	2
c)	Explain the basic Principle of operation of associative, direct and set-associative mappings in cache memory?	4	3	5	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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